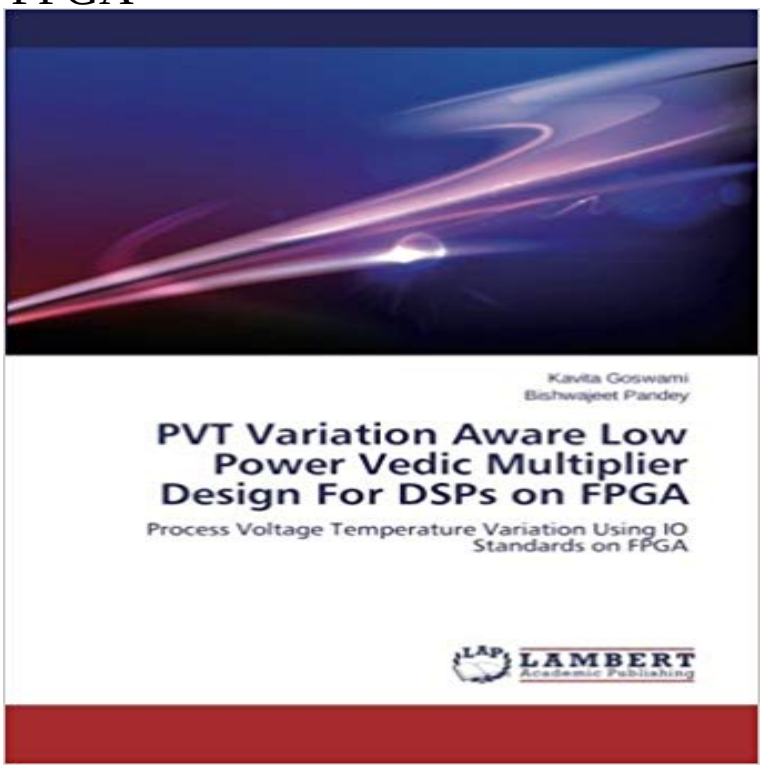
PVT Variation Aware Low Power Vedic Multiplier Design For DSPs on FPGA: Process Voltage Temperature Variation Using IO Standards on FPGA



As the communication and signal processing industries are proliferating the demand for the multipliers is continuously increasing at a rapid rate. For researchers, to develop high speed and power efficient multiplier has been a grave matter of concern. Reduction in the power consumption and delay of a multiplier circuitry is expected to cause a revolution in the field of electronics and communication.The performance of system is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Hence, optimizing the speed and power consumption of the multiplier is a major design issue. There is need of development of high speed and low power multiplier for digital signal processing algorithms. From the previous research, it has been concluded that Vedic multiplier are more efficient than conventional multiplier. In this work, low power Vedic multiplier has been proposed.

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